



Dwyer 7-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Dwyer et al.  
Case: 7-15  
Serial No.: 09/975,762  
Filing Date: October 9, 2001  
Group: 2188  
Examiner: John A. Lane

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Signature: [Signature] Date: November 2, 2004

Title: Method and Apparatus for Reducing Cache Thrashing

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief  
Commissioner of Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Submitted herewith are the following documents relating to the above-identified patent application:

1. Appeal Brief (original and two copies); and
2. Copy of Notice of Appeal, filed on September 2, 2004, with copy of stamped return postcard indicating receipt of Notice by PTO on September 7, 2004.

There is an additional fee of \$340 due in conjunction with this submission under 37 CFR §1.17(c). Please charge **Deposit Account No. 50-0762** the amount of \$340, to cover this fee. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error. A duplicate copy of this letter and two copies of the Appeal Brief are enclosed.

11/05/2004 FHETEKI1 00000008 500762 09975762

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Date: November 2, 2004

Respectfully,

[Signature]

Kevin M. Mason  
Attorney for Applicant(s)  
Reg. No. 36,597  
Ryan, Mason & Lewis, LLP  
1300 Post Road, Suite 205  
Fairfield, CT 06824  
(203) 255-6560



**COPY**

**Ryan, Mason & Lewis, LLP  
ATTORNEYS AT LAW  
1300 POST ROAD  
SUITE 205  
FAIRFIELD, CT 06824**

Receipt in the USPTO is hereby acknowledged of:

Transmittal Letter – (Original & 1 copy)  
Notice of Appeal – (Original & 1 copy)

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Case Name: Dwyer 7-15  
Serial No.: 09/975,762

1150-1032

September 2, 2004 KMM



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**NOTICE OF APPEAL FROM THE EXAMINER TO THE  
BOARD OF PATENT APPEALS AND INTERFERENCES**

Docket Number (Optional)

Dwyer 7-15

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name

Tina Maurice

In re Application of

Dwyer et al.

Application Number

09/975,762

Filed

October 9, 2001

For **Method and Apparatus for Reducing Cache  
Thrashing**

Group Art Unit

2188

Examiner

John A. Lane

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 1.17(b))

\$ 330.00

- ☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is: \$ \_\_\_\_\_.
- ☐ A check in the amount of the fee is enclosed.
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- ☐ The Commissioner has already been authorized to charge fees in this application to a Deposit Account. I have enclosed a duplicate copy of this sheet.
- ☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 50-0762. I have enclosed a duplicate copy of this sheet.
- ☐ A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

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I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest.  
See 37 CFR 3.71. Statement under 37 CFR 3.73(b)  
is enclosed. (Form PTO/SB/96)
- ☒ attorney or agent of record.
- ☐ attorney or agent acting under 37 CFR 1.34(a).  
Registration number if acting under 37 CFR 1.34(a) \_\_\_\_\_.

Kevin M. Mason

Signature

Kevin M. Mason  
Typed or printed name

September 1, 2004  
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below\*.

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Ap/2188-  
JPW

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Patent Application

5 Applicant(s): Dwyer et al.  
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15 APPEAL BRIEF

Mail Stop Appeal Brief - Patents  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

20 Applicants hereby appeal the final rejection dated July 22, 2004, of claims  
1 through 30 of the above-identified patent application.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc., as evidenced by  
25 an assignment recorded on October 9, 2001 in the United States Patent and Trademark  
Office at Reel 012260, Frame 0369. The assignee, Agere Systems Inc., is the real party  
in interest.

RELATED APPEALS AND INTERFERENCES

30 There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1 through 30 are pending in the above-identified patent  
application. Claims 1-30 are rejected under 35 U.S.C. §112, first paragraph, as  
35 containing subject matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1, 10, 19, and 27 remain rejected under 35 U.S.C. §102(e) as being anticipated by Nakamura et al. (United States Patent Application Number 2002/0099912) and claims 2-9, 11-18, 20-26, and 28-30 remain rejected under 35 U.S.C. §103(a) as being unpatentable over Nakamura et al.

### STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

### SUMMARY OF INVENTION

The present invention is directed to a method and apparatus for adaptively decreasing cache thrashing in a cache memory device. Cache performance is improved by automatically detecting thrashing of a set and then providing one or more augmentation frames as additional cache space. In one embodiment, the augmentation frames are obtained by mapping the blocks that map to a thrashed set to one or more additional, less utilized sets. The disclosed cache thrashing reduction system initially identifies a set that is likely to be experiencing thrashing, referred to herein as a thrashed set. Once thrashing is detected, the cache thrashing reduction system selects one or more additional sets to augment a thrashed set, referred to herein as the augmentation sets. In this manner, blocks of main memory that are mapped to a thrashed set are now mapped to an expanded group of sets (the thrashed set and the augmentation sets). Finally, when the augmentation sets are no longer likely to be needed to decrease thrashing, the augmentation set(s) are disassociated from the thrashed set(s).

### ISSUES PRESENTED FOR REVIEW

- i. Whether claims 1-30 are properly rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention;

- ii. Whether claims 1, 10, 19, and 27 are properly rejected under 35 U.S.C. §102(e) as being anticipated by Nakamura et al.; and
- iii. Whether claims 2-9, 11-18, 20-26, and 28-30 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over Nakamura et al.

5

### GROUPING OF CLAIMS

The rejected claims do not stand and fall together. More particularly, for the reasons given below, Applicants believe that each of the dependent claims 5/14/23/29, 6/15/24, 7/16/25, 8/17, and 9/18/26/30 provide independent bases for patentability apart from the rejected independent claims.

10

### ARGUMENT

#### Section 112 Rejections

Claims 1-30 are rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Regarding claims 1, 10, 19, and 27, the Examiner asserts that the claim language “wherein said one or more additional frames and said thrashed set are at the same memory hierarchical level as said cache” is not supported by the specification since the specification does not discuss hierarchical levels or layers.

20

Applicants note that the present invention is directed to methods and apparatus for adaptively decreasing cache trashing in a cache memory device. The cache memory device is a single level cache device, thus a discussion of hierarchical levels or layers in the original specification was unnecessary. Multiple hierarchical levels or layers, however, are well known in the art, as exemplified by the discussion of level 1 cache memory and low-level cache memory in the cited prior art (Nakamura: FIG. 1; page 2, section 16). The cited limitation emphasizes that the cache memory method and apparatus disclosed in the present invention is a single level cache architecture and does not add any new matter.

25

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Thus, the section 112 rejection is believed to be improper and should be withdrawn.

Independent Claims 1, 10, 19 and 27

Independent claims 1, 10, 19, and 27 are rejected under 35 U.S.C. §102(e) as being anticipated by Nakamura et al. In particular, Examiner asserts that the claimed “selector for identifying one or more additional frames” corresponds to circuitry inherently found in Nakamura for selecting/accessing additional sets within cache assist buffer 9, 12 and/or low-level cache memory 11.

In the previous Office Action, Applicants noted that Nakamura discloses an operation that “can transfer line data which has caused thrashing from the cache assist buffer 12 that is *a layer between the level 1 cache memory 23 and the low-level cache memory and main memory 11.*” (Page 3, section 39.) Thus, when the cache assist buffer tag 9 has an entry which has a hit in the comparison with the line address for the line data transfer request, *data is transferred from the associated line of the cache assist buffer 12 to the level 1 cache memory 23* as well as to the load and store unit 1 via the data transfer path 13. (Page 3, section 42.) Independent claims 1, 10, 19, and 27, as amended, require wherein said one or more additional frames and said thrashed set are *at the same cache hierarchical level*. It is noted that the “same memory hierarchical level” as said cache includes frames in the same cache or an equivalent memory hierarchical level.

In the final Office Action, the Examiner contends that Nakamura’s cache assist buffer 12 is essentially at the same hierarchical level as shown in FIG. 1, and that the cache assist buffer 12 is accessed in parallel with level-1 cache memory and substantially simultaneously.

Applicants note that Nakamura, in the text cited above, clearly describes the cache assist buffer 12 as “*a layer between the level 1 cache memory 23 and the low-level cache memory and main memory 11.*” Regarding the assertion that the cache assist buffer 12 is accessed in parallel with level-1 cache memory and substantially simultaneously, Applicants note that Nakamura teaches that

the request of access to data that has been casted out of the level 1 cache memory 23 by thrashing results in a miss-hit in the comparison with data in the level-1-cache-memory tag table 24, and miss-hit information is sent via level-1-cache-memory hit result paths 20 and



21. Based on the miss-hit information, the line data transfer request is transferred to a low-level cache memory and main memory 11 *through line-data transfer request paths 2, 3 and 10.*

Page 2, section 22.

Note that request lines 2 and 3 are utilized to access the cache assist buffer 12, and thus the delay in accessing the cache assist buffer 12 and the delay in accessing the low-level cache memory 11 are both different in comparison to the delay in accessing level 1 cache memory.

Applicants also note that, when a line data transfer request results in transferring data from the cache assist buffer 12, the data is transferred to the *level 1 cache memory* in addition to the load and store unit 1 (page 3, section 42). If the cache assist buffer 12 were at the same hierarchical level as the level 1 cache, it would not be necessary to transfer the data from the cache assist buffer 12 to the level 1 cache. This would only occur if the caches were at different hierarchical levels.

Thus, the cache assist buffer 12 is properly described as being at a different level or layer than the level 1 cache, as would be apparent to a person of ordinary skill in the art.

Thus, Nakamura et al. do not disclose or suggest wherein said one or more additional frames and said thrashed set are at the same cache hierarchical level, as required by independent claims 1, 10, 19, and 27, as amended.

The rejections of the independent claims under §102 in view of Nakamura et al. are therefore believed to be improper and should be withdrawn.

#### Dependent Claims

Claims 5/14/23/29, 6/15/24, 7/16/25, 8/17, and 9/18/26/30 specify a number of limitations providing additional bases for patentability. Specifically, the Examiner rejected claims 5-9, 14-18, 23-26, and 29-30 under 35 U.S.C. §103(a) as being unpatentable over Nakamura et al. Claims 5, 14, 23, and 29 require transforming a set index identifying a set in said cache memory for a block of main memory to an expanded group of sets including said thrashed set and one or more additional sets. Claims 6, 15, and 24 require wherein said selector identifies said one or more additional frames to augment said thrashed set using an access rate of said additional frames. Claims 7, 16,



and 25 require wherein said selector identifies said one or more additional frames to augment said thrashed set using a position in an address space of said additional frames. Claims 8 and 17 require wherein said one or more additional frames are shared with said thrashed set. Claims 9, 18, 26, and 30 require further comprising disassociating said one  
5 or more additional sets from said thrashed set when the additional sets are no longer needed to decrease thrashing.

The Examiner asserts that most, if-not-all, dependent claim features are taught by Nakamura et al. and appear to be well known. Applicant believes that the features of the independent claims cited above are not well known and have not been  
10 disclosed in the prior art, including Nakamura.

Thus, Nakamura et al. and well known prior art, alone or in combination, do not disclose or suggest transforming a set index identifying a set in said cache memory for a block of main memory to an expanded group of sets including said thrashed set and one or more additional sets, as required by claims 5, 14, 23, and 29, do not disclose or  
15 suggest wherein said selector identifies said one or more additional frames to augment said thrashed set using an access rate of said additional frames, as required by claims 6, 15, and 24, do not disclose or suggest wherein said selector identifies said one or more additional frames to augment said thrashed set using a position in an address space of said additional frames, as required by claims 7, 16, and 25, do not disclose or suggest  
20 wherein said one or more additional frames are shared with said thrashed set, as required by claims 8 and 17, and do not disclose or suggest further comprising disassociating said one or more additional sets from said thrashed set when the additional sets are no longer needed to decrease thrashing, as required by claims 9, 18, 26, and 30.

The remaining rejected dependent claims are believed allowable for at  
25 least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,



Date: November 2, 2004

Kevin M. Mason  
Attorney for Applicant(s)  
Reg. No. 36,597  
Ryan, Mason & Lewis, LLP  
1300 Post Road, Suite 205  
Fairfield, CT 06824  
(203) 255-6560

APPENDIX

1. A cache memory, comprising:  
a plurality of sets of cache frames for storing information from main  
5 memory;  
a thrashing detector for determining when one or more of said sets are a  
thrashed set; and  
a selector for identifying one or more additional frames to augment said  
thrashed set, wherein said one or more additional frames and said thrashed set are at the  
10 same memory hierarchical level as said cache.
2. The cache memory of claim 1, wherein said thrashing detector evaluates a  
miss rate of a set.
- 15 3. The cache memory of claim 2, wherein said thrashing detector further  
comprises a miss counter and an access counter.
4. The cache memory of claim 2, wherein said miss rate of a set is  
determined by comparing a number of misses experienced during a given number of  
20 accesses.
5. The cache memory of claim 1, further comprising a mapper that  
transforms a set index identifying a set in said cache memory for a block of main memory  
to an expanded group of sets including said thrashed set and one or more additional sets.  
25
6. The cache memory of claim 1, wherein said selector identifies said one or  
more additional frames to augment said thrashed set using an access rate of said  
additional frames.

7. The cache memory of claim 1, wherein said selector identifies said one or more additional frames to augment said thrashed set using a position in an address space of said additional frames.

5 8. The cache memory of claim 1, wherein said one or more additional frames are shared with said thrashed set.

9. The cache memory of claim 1, further comprising a mechanism for disassociating said one or more additional sets from said thrashed set when the additional  
10 sets are no longer needed to decrease thrashing.

10. A method for reducing thrashing in a cache memory, said method comprising the steps of:

15 storing information from main memory in a plurality of sets of cache frames;

detecting when one or more of said sets are a thrashed set; and

identifying one or more additional frames from said plurality of sets to augment said thrashed set, wherein said one or more additional frames and said thrashed set are at the same memory hierarchical level as said cache.

20

11. The method of claim 10, wherein said detecting step further comprises the step of evaluating a miss rate of a set.

12. The method of claim 11, wherein said miss rate is obtained using a miss  
25 counter and an access counter.

13. The method of claim 11, wherein said miss rate of a set is determined by comparing a number of misses experienced during a given number of accesses.

14. The method of claim 10, further comprising the step of transforming a set index identifying a set in said cache memory for a block of main memory to an expanded group of sets including said thrashed set and one or more additional sets.

5 15. The method of claim 10, wherein said identifying step further comprises the step of identifying said one or more additional frames to augment said thrashed set using an access rate of said additional frames.

16. The method of claim 10, wherein said identifying step further comprises  
10 the step of identifying said one or more additional frames to augment said thrashed set using a position in an address space of said additional frames.

17. The method of claim 10, wherein said one or more additional frames are shared with said thrashed set.

15

18. The method of claim 10, further comprising the step of disassociating said one or more additional sets from said thrashed set when said additional sets are no longer needed to decrease thrashing.

20 19. A cache memory, comprising:  
means for storing information from main memory in a plurality of sets of cache frames;  
means for detecting when one or more of said sets are a thrashed set; and  
means for identifying one or more additional frames from said plurality of  
25 sets to augment said thrashed set, wherein said one or more additional frames and said thrashed set are at the same memory hierarchical level as said cache.

20. The cache memory of claim 19, wherein said means for detecting thrashing evaluates a miss rate of a set.

30

21. The cache memory of claim 20, wherein said means for detecting thrashing further comprises means for counting frame misses counter and frame accesses.

22. The cache memory of claim 20, wherein a miss rate of a set is determined  
5 by comparing a number of misses experienced during a given number of accesses.

23. The cache memory of claim 19, further comprising means for transforming a set index identifying a set in said cache memory for a block of main memory to an expanded group of sets including said thrashed set and one or more  
10 additional sets.

24. The cache memory of claim 19, wherein said means for identifying identifies said one or more additional frames to augment said thrashed set using an access rate of said additional frames.

15 25. The cache memory of claim 19, wherein said means for identifying identifies said one or more additional frames to augment said thrashed set using a position in an address space of said additional frames.

20 26. The cache memory of claim 19, further comprising means for disassociating said one or more additional sets from said thrashed set when the additional sets are no longer needed to decrease thrashing.

27. An integrated circuit, comprising:

25 a cache memory having a plurality of sets of cache frames for storing information from main memory;

a thrashing detector for determining when one or more of said sets are a thrashed set; and

a selector for identifying one or more additional frames to augment said  
30 thrashed set, wherein said one or more additional frames and said thrashed set are at the same memory hierarchical level as said cache.

28. The integrated circuit of claim 27, wherein said thrashing detector evaluates a miss rate of a set.

5 29. The integrated circuit of claim 27, further comprising a mapper that transforms a set index identifying a set in said cache memory for a block of main memory to an expanded group of sets including said thrashed set and one or more additional sets.

30. The integrated circuit of claim 27, further comprising a mechanism for  
10 disassociating said one or more additional sets from said thrashed set when the additional sets are no longer needed to decrease thrashing.